UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

21967 7590 05/28/2009

HUNTON & WILLIAMS LLP
INTELLECTUAL PROPERTY DEPARTMENT
1900 K STREET, N.W.
SUITE 1200
WASHINGTON, DC 20006-1109

EXAMINER	
TAYLOR, EARL N	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 05/28/2009

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/553,470	05/19/2006	Ralf Lerner	60291.000041	8935

TITLE OF INVENTION: MONITORING THE REDUCTION IN THICKNESS AS MATERIAL IS REMOVED FROM A WAFER COMPOSITE AND TEST STRUCTURE FOR MONITORING REMOVAL OF MATERIAL

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	08/28/2009

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

21967 7590 05/28/2009

HUNTON & WILLIAMS LLP
INTELLECTUAL PROPERTY DEPARTMENT
1900 K STREET, N.W.
SUITE 1200
WASHINGTON, DC 20006-1109

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/553,470	05/19/2006	Ralf Lerner	60291.000041	8935

TITLE OF INVENTION: MONITORING THE REDUCTION IN THICKNESS AS MATERIAL IS REMOVED FROM A WAFER COMPOSITE AND TEST STRUCTURE FOR MONITORING REMOVAL OF MATERIAL

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	08/28/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
TAYLOR, EARL N	2818	257-048000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/553,470	05/19/2006	Ralf Lerner	60291.000041	8935

21967 7590 05/28/2009

HUNTON & WILLIAMS LLP
INTELLECTUAL PROPERTY DEPARTMENT
1900 K STREET, N.W.
SUITE 1200
WASHINGTON, DC 20006-1109

EXAMINER	
TAYLOR, EARL N	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 05/28/2009

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

Notice of Allowability	Application No.	Applicant(s)	
	10/553,470	LERNER, RALF	
	Examiner	Art Unit	
	EARL N. TAYLOR	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *papers filed 17 March 2009*.

2. ☒ The allowed claim(s) is/are *1-9,13,14 and 17-24*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Steven Loke/
Supervisory Patent Examiner, Art Unit 2818

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Patrick Edwards, Reg. No. 57650 on 20 May 2009.

Amend the specification at indicated paragraph numbers as shown (additions are underlined and deletions are strikethrough):

[0001] This application is a U.S. National Phase of International Application No. PCT/DE2004/000801, filed April 16, 2004~~, which claims priority to German 103 17 747.7, filed April 17, 2003. The entire contents of all the above identified applications are incorporated herein by reference~~.

[0003] US 6,242,320 (Sang Mun So) discloses differently deep trenches formed in a first wafer. A second wafer is also used. The trenches have alternating depths; a deeper trench is positioned between two shallower trenches. By means of two successive polishing steps illustrated in this document in Figs. ~~26 and 21~~ 2G and 2I, cf. column 4, lines 8 to 51, a uniform thickness of the upper wafer is achieved. The trenches are filled with an insulating material, cf. column 3, lines 20 to 29, acting as "polishing stops",

associated with an intermediate etch process, in which the deeper trenches (indicated as 25) are etched down to a depth corresponding to the less deep trenches (indicated as 23), cf~~,~~. Fig. 2H of this document.

[0004] US 6,156,621 (Nance et al., Infineon) discloses a method for manufacturing a ~~Si-Si02-Si~~ silicon–silicon oxide–silicon wafer, wherein initially isolation trenches (trenches) are provided in a homogeneous silicon wafer that is subsequently bonded with its surface to a second wafer. A conductive layer of polysilicon, indicated as 9 in this document, is located between the ~~25~~ two wafers (2 and 3), which fills the trenches and also forms a connecting intermediate layer (indicated as 9, 4) between the two wafers ~~(indicated as 9, 4)~~. After grinding (thinning) the front side the isolation trenches may be exposed; the thinning process is performed prior to bonding this wafer to the polysilicon layer in order to form the wafer composite, cf. column 3, lines 18 to 23, or the German counter part DE 197 41 971, column 2, lines 31 to 39. The ~~30~~ result is a double wafer including isolation trenches. Due to the influence of the support layer (i.e., the polysilicon layer 4) and to the risk of lattice defects and interferences as well as contaminations of the polished surface during a control measurement monitoring of the grinding and polishing thickness is difficult.

[0005] Depth measurements based on by step structures and conical configurations are disclosed in US 6,514,858 (Hauser et al., AMD), cf. Figs. ~~.$A~~ 4A, 4B and 3C. During the removal process the width of the trenches increases, wherein the filling in was

accomplished by means of a metal, which may optically be detected on the basis of its change in width in a step-like or continuous manner. The formation of trenches having a conically configured sidewall structure is technically difficult and is accompanied with an affording necessary measurement procedure on the semiconductor.

[0007] According to the present invention the object is solved by a test structure ~~(claim 10)~~ used in the context of a method ~~(claim 1)~~. By this (efficient) test structure a system of trenches is determined, which may be used at least for a coarse determination of the amount of removal or removal depth.

[0008] The trenches are disposed in a systematic row. They are provided in a first wafer that is also referred to as device wafer (or active wafer) due to its function of receiving, after the reduction in thickness, active devices such as semiconductors or circuits in one or more later manufacturing processes ~~(claim 5)~~.

[0009] The passive wafer is the carrier wafer, which may be an insulating wafer ~~(claim 6)~~. The two wafers are bonded together by means of a bond connection acting as an area-like connection.

[0010] The systematic row of trenches defines a system of trenches of determined yet different depth, which are arranged in a sequence. The trenches and their different depths are obtained by etching on the basis of etch mask openings of a mask ~~(claim 3)~~.

By means of this etch process trenches of different width and thus different depth ~~(claims 2, 3)~~ are formed in the active wafer. The active wafer later receives the active electronic circuitry, ~~which is the~~ giving reason for its name "active wafer".

[0011] The amount or the removal depth during the material removal from the wafer, obtained for instance by polishing or lapping, is controlled on the basis of a desired (target) thickness of the active wafer, which is to be determined in advance ~~(claim 13)~~. When the desired reduction in thickness is achieved the removal process may be terminated ~~(claims 9, 14)~~. In order to detect the end point of the removal process optical means are used for observing the process to monitor the reduction in thickness. To this end, a trench depth is assigned to the target thickness, that is, a trench from the systematic row is selected or determined in advance as a reference trench whose depth at least substantially corresponds to the desired thickness of the active wafer.

[0012] Unless one of the trenches located at the periphery is selected the reference trench is flanked by one less deep (shallower or flatter) trench and one deeper trench. Flanking is to be understood such that the trenches are ~~neighbours~~ neighbors of the reference trench~~, i.e., they~~. They are spaced apart yet are located not too far from the reference trench.

[0013] The process of selecting one of the trenches as a reference trench as described above may be performed in a later stage, after the active wafer and the carrier wafer are

bonded together. To this end, the trenches are bonded upside down, that is, with their open or upper side facing downwards, onto the surface of the carrier wafer. The top side is the side on which the test structure is located, that is, the surface in which the systematic row of the plurality of trenches has been formed. This side is bonded to the carrier wafer ~~(claim 4)~~.

[0014] When in the process of the wafer treatment the material removal is performed in the active wafer, that is, on the backside of the active wafer, the thickness thereof is reduced. This material removal is continued until the reference trench is visible from the ~~20~~ backside of the active wafer~~, i.e., its~~. The bottom thereof is exposed, that is, this trench is visible at all. This is detected by the observation means.

[0018] If, for example, a removal process for exposing one of the trenches of the systematic row previously formed in the active wafer is considered, the test structure may be configured such that the desired depth of the isolation trench of the wafer is located in the central region of the row of the differently deep trenches~~, i.e.,~~. The trench indicating the desired depth is flanked by trenches of less depth and trenches of increased depth ~~(claim 1, claim 15)~~.

[0019] During the formation of the trenches in the active wafer a respective reference trench of the test structure is formed with the same depth when having the same width as a ~~lo~~ different trench. The broader trenches automatically result in an increased depth

during etching, while the narrower trenches result in a reduced depth, cf. US 6,515,826 B1 (Hsiao, IBM), abstract and Figs. 15 and 16~~, with emphasis~~ thereof, emphasizing on the progression of the trench depth vs. the opening width.

[0027] Fig. I is a cross-sectional view. Reference numeral 1 represents an insulating layer, for example, a carrier wafer made of silicon dioxide~~, Si02~~. The active layer 2 is made of, for instance, silicon. It is also referred to as semiconductor layer or device wafer. The top side 2b' of the active layer 2 is depicted in an already thinned state so that three trenches of the plurality of trenches 4, 5, 6, 7, 8, 9 are already opened. The other three trenches are still closed. The wafer has a height ~~h6~~ h_6 that substantially corresponds to the depth of the trench 6 having a width ~~b6~~ b_6. Respective widths ~~b4~~ b_4 to ~~b9~~ b_9 correspond to the trenches 4 to 9, respectively.

[0031] In Fig. 2a there is shown an example of a semiconductor wafer 2 not yet applied to the insulating layer 1 in an upside down configuration is. Here the same trenches as in Fig. 1 are shown that have different width and different depth, while the semiconductor wafer 2 is still thicker. It has a basic thickness ~~ho~~ h_0. Trenches are formed in the semiconductor wafer 2, which form as trenches 4 to 9 a systematic row, ordered by depth and width, wherein during the etch process that is not explicitly shown the broad trenches automatically receive a greater depth as may be appreciated by the skilled person. The trench 4 has the greatest depth and the greatest width. The trench 9

has the smallest depth and the smallest width.

[0033] Hence, the device wafer 2 has two height sections, that is, the section 2d, in which the trenches are formed, and a further section 2c, which has no trenches formed therein. Both sections are commonly applied to the second wafer 1 of the wafer pair, using the top sides 2a, i.e., the side from which the test structure was formed. This second wafer ~~1~~ may be an insulating layer, formed of, for instance, silicon dioxide. A bonding process is performed in which both wafers are firmly connected to each other.

[0034] The result of the removal of the section 2c of the device wafer is shown in Fig. 1 for the case that the removal was performed to such a depth that ~~h0~~ h_0 is reduced to ~~h6~~ h_6 in order to just expose the trench bottom 6a and to make the trench 6 of width 6b visible for the optical device 30. In this state the surface 2b is reduced compared to the remaining surface 2b', as shown in Fig. 1.

[0035] The trench 6 is located substantially in the central region of the row of trenches 4 to 9, so that at both sides thereof trenches are provided, which systematically become deeper and shallower, respectively, From this, a description of a systematic row of trenches results, which has a different depth and is located in the active wafer that is to receive an active electronic circuit in a later stage. The desired thickness ~~h6~~ h_6 is the target thickness or the target value, to which the thickness is to be reduced. This thickness aimed at as a target value substantially corresponds to the depth t6 of the

trench 6. The more frequently the removal process is interrupted in order to detect the exposure of the reference trench 6 by means of the measurement device 30, the more accurately the removal process may be controlled. Since the reference trench is flanked by at least one deeper trench and at least one shallower trench, that is, these trenches are arranged in parallel, the reduction in thickness with respect to the vertical direction may be mapped to the visible plane.

[0038] Fig. 2b illustrates a further embodiment, which shows a perform of the result of Fig. 1. The same reference numerals are used so as to maintain conciseness of the 20 description while nevertheless providing a more detailed understanding. Applying the embodiment of Fig. 2a with its top side 2a to the top side ~~1 a~~ 1a of the insulating layer 1 yields an ~~SO1~~ SOI structure with all the trenches 4 to 9 still closed. The respective trenches may become visible upon performing the removal process from the side 2b. The opposing side of the wafer composite formed from bonded wafers is lb and forms the bottom side for this process step. Here the bonded wafer is supported.

[0044] At reference trench 7 the bottom 7a is concerned, that is, the narrower and less deep trench 7 having the depth ~~t7~~ t_7. When the removal height is increased to $h_0 - t_7$, first the trench 6 is exposed, and during the further removal process trench 7 is exposed, too, which may also be detected by the optical device 30.

[0047] All trenches are recognizable as stripe-like trenches each having a ~~length l and a width b~~ length and width. For example, the trench 5 had a length l5, ~~15,~~ the trench 4 has a width ~~b4~~ b_4. Respective characteristics also apply to all other trenches. The length is greater compared to the width, but in the systematic row the width decreases as the depth of the trenches 4 to 9 should decrease.

[0049] This state having the removed height ~~h7~~ h_7 of the device wafer 2 is shown in Fig. 3b in a cross-sectional view.

Amend the claims as shown:

Claim 1 recites “neighboured” and should read --neighbored--.

Cancel claims 10-12, 15 and 16

Claim 19 recites “neighbouring” and should read --neighboring--.

Claim 24 recites “neighboured” and “neighbouring” and should read --neighbored-- and neighboring-- respectively.

Allowable Subject Matter

Claims 1-9, 13, 14, 17-24 are allowed.

The following is an examiner's statement of reasons for allowance:

Regarding Claim 1, the prior art of record alone or in combination neither teaches nor makes obvious the invention of performing the wafer material removal, commencing from a backside of the bonded active wafer until the reference trench is exposed and optically detecting said exposure of the reference trench, for monitoring a thickness reduction of the active wafer; and wherein a targeted thickness of the active wafer after a removal of wafer material corresponds at least substantially to a reference depth of a reference trench in the row of trenches in said test structure, said reference trench neighbored by a shallower and a deeper trench; forming at least one active circuit in said active wafer in said later step in combination with all of the limitations of Claim 1.

Regarding Claim 24, the prior art of record alone or in combination neither teaches nor makes obvious the invention of performing a wafer material removal comprising a polishing process, commencing from a backside of the bonded active wafer until a reference trench is exposed, and optically detecting the exposure for monitoring thickness reduction of the active wafer down to a target thickness; and forming an active circuit in said active wafer in said later step; wherein the target thickness of the active wafer upon said material removal corresponds to a depth of said reference trench of the row of trenches in said test structure, said reference trench neighbored by a shallower and a deeper trench in combination with all of the limitations of Claim 24.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Telephone / Fax Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Earl N. Taylor whose telephone number is (571) 272-8894. The examiner can normally be reached on Monday-Friday from 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on (571) 272-1657. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner: Earl N. Taylor

/Steven Loke/
Supervisory Patent Examiner, Art Unit 2818